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REMARKS

Claims 15-34 are all of the claims pending in the application. Claims 15, 21, and 29 stand rejected under 35 U.S.C. 112, first paragraph; and claims 15-34, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 U.S.C. §112, First Paragraph, Rejection

Claims number 15, 21, and 29 stand rejected under 35 U.S.C. §112, first paragraph. The Office Action argues that the recently added limitation "said uppermost layer maintains performance of said semiconductor device irrespective of resistivity shifts" is not supported by the specification. In response thereto, Applicants directs the reader's attention to page 6, lines 4-12 of the application. There, the application clearly states that the last metalization layer comprises very thick metallurgy and it is, therefore, substantially less sensitive to resistivity shifts that are associated with the extra thick silicide layer. This clearly supports the added claim language. Therefore, it is Applicants' position that the added claim language is fully supported by the specification and that the 35 U.S.C. § 112, first paragraph rejection should be withdrawn. Notwithstanding the above, the offending limitation has been removed, in order to render this rejection moot and speed prosecution. In addition, new language which substantially mirrors the language in the specification is added, above, to the claims to further define the invention. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 15-18, 21-24, and 27-32 stand rejected under 35 U.S.C. §103(a) as being anticipated by Filipiak (U.S. Patent No. 5,447,887), hereinafter "Filipiak," and claims

19-20, 25-26, and 33-34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Filipiak in view of Dass et al. (U.S. Patent 6,046,101) hereinafter "Dass." Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Filipiak

1. The Position in the Office Action

The Office Action admits that Filipiak does not teach that the silicide thickness should be in the range of 10% to 20%, as defined by independent claims 21 and 29. However, the Office Action argues that the silicide thickness can be changed depending upon the application of the device and that up to the entire thickness of the layer could silicided (and cites column 5, line 63-column 6, line 6 of Filipiak as support for such arguments).

2. The Filipiak Reference

Filipiak discloses that a silicon nitride layer (34) has improved adhesion to underlying copper interconnect members (30) through the incorporation of an intervening copper silicide layer (32). Layer (32) is formed in-situ with a plasma enhanced chemical vapor deposition (PECVD) process for depositing a silicon nitride layer (34). To form layer (32), a semiconductor substrate (12) is provided having a desired copper pattern formed thereon. The copper pattern may include copper interconnects, copper plugs, or other copper members. The substrate is placed into a PECVD reaction chamber. Silane is introduced into the reaction chamber in the absence of a plasma to form a copper silicide layer on any exposed copper surfaces. After a silicide layer of a sufficient thickness (for example, 10 to 100 angstroms) is formed, PECVD silicon nitride is deposited. The copper silicide layer improves adhesion such that the silicon nitride layer is less prone to peeling away from underlying copper members.

3. Applicants' Response

The disclosure in Filipiak is consistent with the description of the problems associated with the prior art (see page 2, lines 5-15 of the application). More specifically, the prior art teaches that the thickness of a silicide layer should not exceed 10% of the total thickness of the metal layer. Filipiak is consistent with this teaching where it states that the thickness of the silicide layer 32 should not be greater than 10% of the total thickness of the copper interconnects as shown in Figure 5 (column 5, line 62-66). Filipiak explicitly explains that the reason for limiting the thickness of the silicide layer to less than 10% of the total copper thickness is that the silicidation degrades the resistivity of the copper interconnect (column 5, line 66-column 6, line 1). Filipiak states that where resistivity is not an important issue silicide thickness may not be as tight the controlled.

In the claimed invention, the thickness of the uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface. Therefore, in the claimed invention, resistivity is an important issue in that reducing sensitivity to resistivity shifts is a claimed feature. Therefore, with respect to the claimed invention (e.g., where resistivity is an important issue), the teachings in Filipiak require that the silicide layer not be greater than 10% of the total thickness of the interconnect.

Contrary to the teachings in Filipiak, independent claims 21 and 29 defined that the silicide surface is within the top 10-20% of the conductive layer. Therefore, since the claims define that resistivity is an important issue and that the silicide surface is outside the range required by Filipiak, Filipiak cannot be said to teach or suggest the invention.

With respect to the arguments in the Office Action that one ordinarily skilled in the art would have experimented outside the 10% range in order to arrive at Applicants' invention, Applicants note that Filipiak teaches one ordinarily skilled in the art not use a silicide thickness greater than 10%. Therefore, using the teachings in Filipiak, one ordinarily skilled in the art

would not use a silicide layer of having a thickness greater than 10% where resistivity shifts are important (as in the claimed invention). The claimed invention breaks away from conventional teachings and includes a silicide layer in the range of 10-20%. Filipiak teaches away from the claimed invention by teaching that the silicide layer should not be greater than 10% in situations where resistivity is important. Therefore, the arguments in the Office Action that Applicants merely discovered an optimum working range involving only routine skill are inappropriate considering that the prior art (Filipiak) teaches one ordinarily skilled in the art not to use ranges above 10% when resistivity issues are important.

Therefore, with respect to claims 21 and 29, that define a silicided surface in the upper 10% to 20% of the bonding pad, Applicants submit that such features are clearly not taught or suggested by Filipiak. Indeed, Filipiak teaches away from such claimed features. In addition, with respect to independent claim 15, Applicants submit that Filipiak does not teach or suggest that the thickness of the uppermost layer reduces resistivity shifts associated with the silicide portion. Applicants resolved resistivity issues according to the thickness of the uppermost layer. To the contrary, Filipiak teaches that one should limit the thickness of the silicide portion in order to control resistivity issues. Therefore, it is also Applicants position that Filipiak teaches away from the claimed invention define by independent claim 15.

Thus, as shown above, Filipiak teaches away from the invention defined by independent claims 15, 21, and 29. Therefore, the invention defined by independent claims 15, 21, and 29 is patentable over Filipiak. Further, dependent claims 16-18, 23-24, 28, and 30-32 are similarly patentable over Filipiak, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Filipiak in view of Dass

1. The Position in the Office Action

With regard to claims 19-20, 25-26, and 33-34, the Office Action states that Filipiak teaches all claimed structure, as applied to claims 15, 21, & 29 above, except the tin solder terminal electrically connected to the bonding pad. However, the Office Action asserts that Dass teaches in Fig. 21 the solder terminal (270) connected to the bonding pad and a silicon nitride (245) including an opening. The Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solder terminal in order to facilitate an electrical connection of the semiconductor structure with an external connector, such as a modulator package substrate.

2. The Dass Reference

Dass discloses an integrated circuit passivation layer including a first passivation layer portion of silicon nitride treated with nitrous oxide and a second passivation layer portion of polymide. Also, a method of passivating an integrated circuit wafer including depositing a first passivation layer over the top surface of an integrated circuit wafer having a scribe street area between adjacent integrated circuit device portions, depositing a second passivation layer over the first passivation layer, and patterning the first passivation layer and the second passivation layer to expose the scribe street area.

3. Applicants' Response

The Dass reference is only utilized in the Office Action to show the use of tin solder when connecting to a bonding pad. Dass is silent regarding siliciding the upper layer of the bonding pad. Therefore, Dass does not cure the deficiencies of Filipiak as discussed above. Thus, even if one ordinarily skilled in the art had combined Dass and Filipiak, the proposed combination would not teach or suggest the invention as defined by independent claims 15, 21, and 29, as discussed above. Therefore, these independent claims are patentable over the proposed combination of references. Further, dependent claims 19-20, 25-26, and 33-34 are similarly patentable thought, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, Applicants respectfully request that the Examiner reconsider and withdraw this rejection.

III. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 15-34, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

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Please charge any deficiencies in fees and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 9/5/02

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Attachment

Marked up Version of Changes Made

15. (Amended) A semiconductor device having at least two levels of interconnecting metallurgy, said semiconductor device comprising:

a first level of substantially silicide free metallurgy; and

an uppermost layer of metallurgy including a bonding pad, wherein a top of said uppermost layer comprises a silicided surface,

[wherein said uppermost layer maintains performance of said semiconductor device irrespective of resistivity shifts]

wherein a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface.

21. (Amended) A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

[and]

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,

[wherein said silicided surface maintains performance of said semiconductor device irrespective of resistivity shifts] and

wherein a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface.

29. (Amended) A semiconductor chip comprising:

an exterior surface having a top level of metallurgy; and

an interior having at least one internal level of metallurgy,

wherein said top level of metallurgy is thicker than said internal level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

[and]

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,

[wherein said silicided surface maintains performance of said semiconductor device irrespective of resistivity shifts] and

wherein a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface.